Notice of Allowability	Applicati n No.	Applicant(s)	
	10/812,766	KIDA ET AL.	
	Examiner	Art Unit	
	Eric W Thomas	2831	Jan J
The MAILING DATE of this communication apperall claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this or other appropriate communica GHTS. This application is subje	application. If not includation will be mailed in due	ed course. THIS
1. X This communication is responsive to the papers filed on 3/1	<u>29/04</u> .		
2. ☑ The allowed claim(s) is/are <u>1-18</u> .			
3. 🗵 The drawings filed on 29 March 2004 are accepted by the	Examiner.		
4.	been received. been received in Application Notuments have been received in the communication to file a reserved. The communication to file a reserved. The communication to file a reserved in the communication to file a reserved. The communication	his national stage applicately his national stage applicately ply complying with the research terms of the control of the cont	quirements NOTICE OF
Attachment(s) 1. ⊠ Notice of References Cited (PTO-892) 2. □ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 3/04 4. □ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summa Paper No./Mail 8), 7. ☑ Examiner's Ame	Date	owance

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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the abstract, line 1, change "comprises" to -having--.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. The following is an examiner's statement of reasons for allowance: The prior art does not teach or fairly suggest (taken in combination with the other claimed features) a chip-type solid electrolytic capacitor having a mounting surface comprising an anode terminal including two branch end portions, respectively, which are formed by shaping, the branch end portions overlap each other by rotation of 180° around a straight line at an intermediate portion between the anode lead wires, the branch portions being welded to the anode lead wires to produce welded portions (claims 1-5); a chip-type solid electrolytic capacitor having a mounting surface comprising an anode terminal including three branches having a first, a second, and a third branch end portion, respectively, which are formed by shaping, the first and the third branch end portions having shapes so as to overlap each other by rotation of 180° around a straight line, the

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second branch end portion being between the first and the third branch end portions, the first, the second, and the third branch end portions being welded to the anode lead wires to produce welded portions (claims 6-10); a chip-type solid electrolytic capacitor having a mounting surface comprising an anode terminal including an anode terminal including four branches having a first, a second, a third, and a fourth branch end portion, respectively, which are formed by shaping, the first and the fourth branch end portions having shapes so as to overlap each other by rotation of 180° around a straight line, the second and the third branch end portions being between the first and the fourth branch end portions and having shapes so as to overlap each other by rotation of 180° around the straight line, the first, the second, the third, and the fourth branch end portions being welded to the anode lead wires to produce welded portions (claims 11-15); a method of producing a chip-type solid electrolytic capacitor wherein preparing a lead frame having an anode terminal forming portion and a cathode terminal forming portion, the anode terminal having a center line and a plurality of branches symmetrical with each other with respect to the center line shaping the branches by bending. welding the capacitor elements to the anode terminal forming portion (claim 16); and a chip type solid electrolytic capacitor comprising a plurality of anode lead wires led out from the capacitor portion in parallel to the mounting surface, the anode lead wires being portioned apart from each other in the predetermined direction, the anode terminal including a plurality of branch end portions which are positioned apart from each other in the predetermined direction and welded to the anode lead wires (claims 17-18).

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3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,343,004 – discloses a solid electrolytic capacitor comprising multiple solid electrolytic capacitor elements connected together via a single terminal member.
6,392,869 – discloses a solid electrolytic capacitor comprising multiple solid electrolytic capacitor elements connected together via anodic elastic body.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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